EMC Fact Sheet 6

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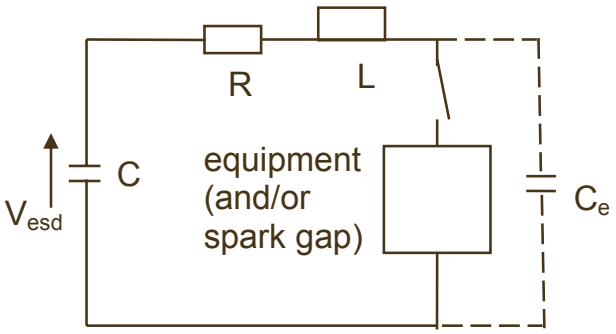
Achieving Electrostatic Discharge (ESD) immunity by design

ESD sources

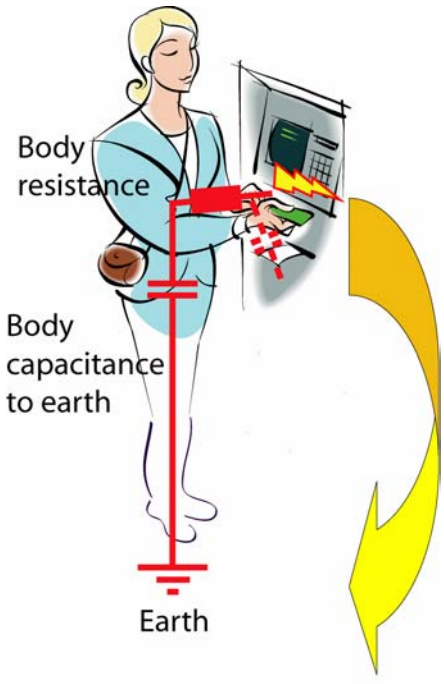


ESD sources have at least three basic elements; a storage capacitor C; series resistance R; series inductance L (R and L may be stray components of the interconnects).

Example: Person using ATM

- Charge is stored on the body capacitance
- Discharge occurs to the ATM
- The ESD current returns to earth by the easiest route

Where does the current go??

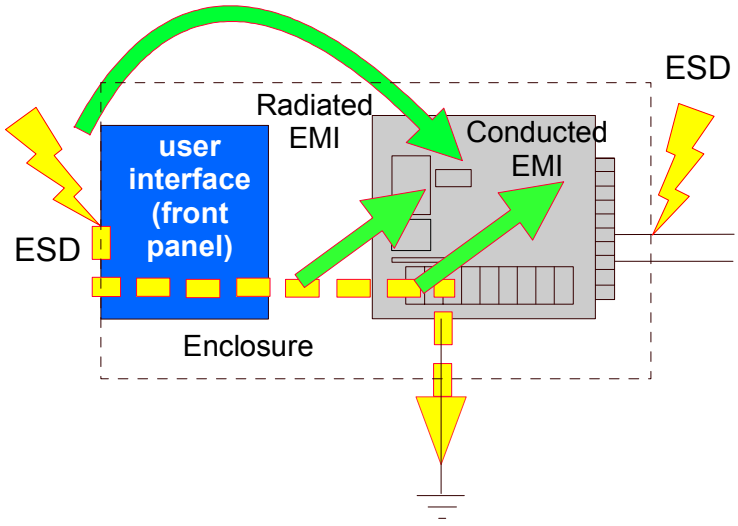


How ESD affects a system

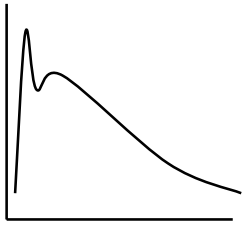
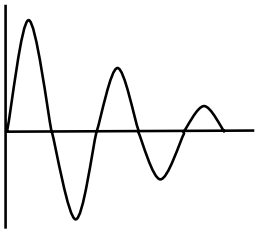
If ESD flows through the system there is a risk of a problem.

Therefore the task is to:

- Anticipate typical ESD sources
- Manage the ESD current flow
- Reduce conducted EMI to insignificant level
- Reduce radiated EMI to insignificant level



ESD waveform characteristics

Human body ESD			
A person gets charged up from walking, sitting or doing anything ! ESD occurs when they touch another conductor such as an equipment panel, chassis, trunking or machine parts.		C=100 – 300 pF R= 0.1 – 100 k Ω L=stray	Rise time ~10 ns Duration ~100ns Frequencies up to GHz Peak current ~0.3 A @ 500V ~7 A @ 10 kV
ESD from larger charged metallic parts			
A tool or machine part gets charged e.g, insulated metal objects or trolleys. ESD occurs when it touches another conductor.		C=10's -100's pF R=stray L=stray	Rise time ~10 ns or less Duration ~100ns or less Frequencies up to GHz Peak current ~8 A @ 500 V
ESD from small charged metallic parts			
A device gets charged through packaging or handling ESD occurs when charged part touches a conductor		C= a few pF R=stray L=stray	Rise time ~0.1 ns Duration ~1ns Frequencies to > GHz Peak current ~14 A @ 500 V

Key ESD features

Feature	Characteristics	Typical values
High dV/dt	Source collapses from kV to near zero in nanoseconds	1 kV in 1 ns = 1012 V/s
High peak current	Tens of Amps possible	
High dI/dt	Tens of amps in nanoseconds	10 A in 1 ns = 1010 A/s

How systems react to ESD

Components and wiring at high frequencies.

Small stray inductances have high impedance and small capacitances have low impedance. Chassis parts and ground wires have inductance and cannot be considered to be at zero volts. Wires and tracks act as antennas and transmission lines.

Small capacitances at high frequencies.

All metalwork, wires and tracks have a capacitance *C* to nearby conductors and components also have stray capacitances inherent in their construction. The impedance Z_C of a capacitor reduces with increasing frequency *f*.

$$Z_c = \frac{1}{2\pi fC}$$

Even very small capacitances have low impedance above a few hundred MHz. This means that the small capacitances between tracks can easily cause coupling across tracks at high frequencies.

Another way of seeing capacitance is to consider the effect of high dV/dt. A transient current *I* flows in a capacitor as a result of a fast changing voltage *V.*

$$C\frac{dV}{dt} = \frac{dQ}{dt} = I$$

This shows that the high dV/dt will inject a charge pulse (current transient) through the small capacitance.

Capacitive coupling

A high impedance E-field couples most effectively with high impedance circuits and high impedance E-field coupling can be considered to be capacitive coupling. Coupling is reduced by reducing the effective capacitance which can be achieved by reducing size of receptor (length of track, area), increasing separation and reducing dielectric constant of materials separating source and receptor.

Inductance at high frequency

All wires, component leads and tracks have some inductance *L*. The inductive impedance *ZL* increases with increasing frequency *f* and often becomes significant. $Z_L = 2\pi fL$

Even a short track can look like a high impedance at high frequencies

Another way of seeing inductance effects is as a transient voltage *V* developed across an inductance as a result of a fast changing current *I* .

$$V = -L\frac{dI}{dt}$$

All conductors have inductance so a high dI/dt transient can cause significant voltage impulses on any conductor – even ground tracks or chassis parts.

Magnetic coupling

A low impedance H-field couples most effectively with low impedance circuits and low impedance H-field coupling can be considered magnetic coupling. Coupling can be reduced by reducing the effective mutual inductance between the source and the receptor e.g. reducing the area of source and receptor circuit loops and increasing separation.

Designing for ESD immunity

EMC design needs a holistic approach and the best ESD immunity will involve many disciplines:-

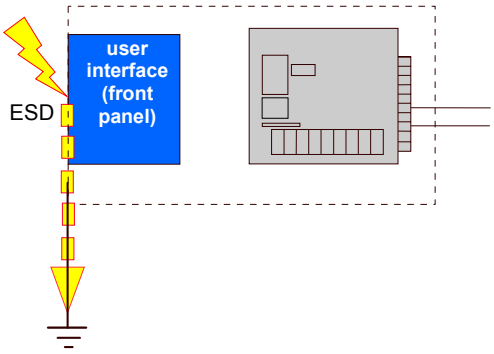
- ESD ground paths
- Enclosure
- Circuit design
- PCB design and layout
- Software design
- System wiring and interconnects

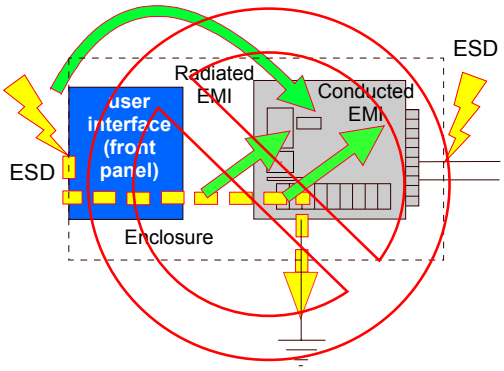
A combined view of the options and interplay of these different aspects will be required to achieve good ESD immunity.

ESD ground paths

ESD Entry points - ESD can inject fast transients into a panel control, keyboard, switch, connector, component or a PCB. Any wire, metal part or ground plane can take EMI into, or out of, a system. Wires leading to, or from, a PCB can conduct EMI into or out of a board. Wires and tracks act as antennas to receive or radiate EMI.

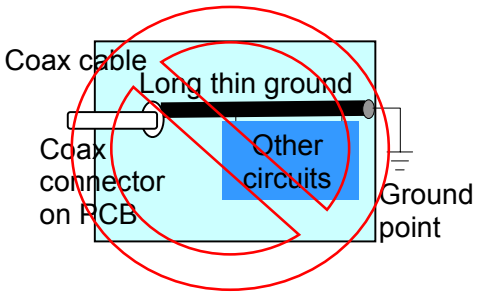
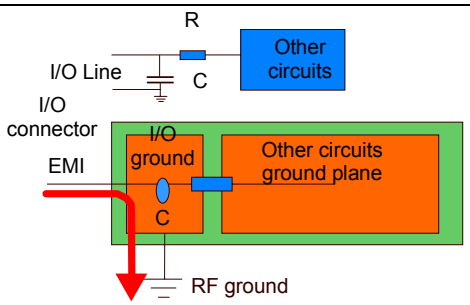
Design ESD Ground paths - Where possible provide a direct ground path to keep the ESD current outside the system. Ideally this should be as short as possible with a low inductance. Don't take the ESD through circuit boards or EMI sensitive regions.

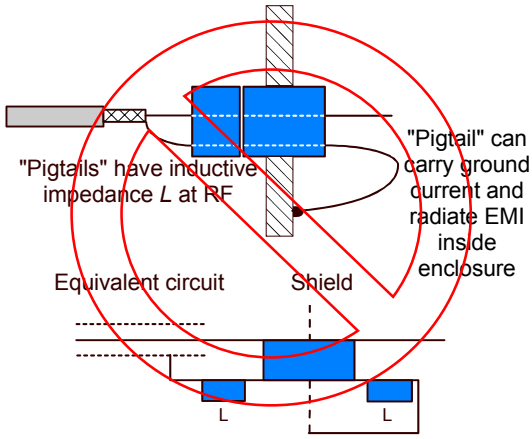
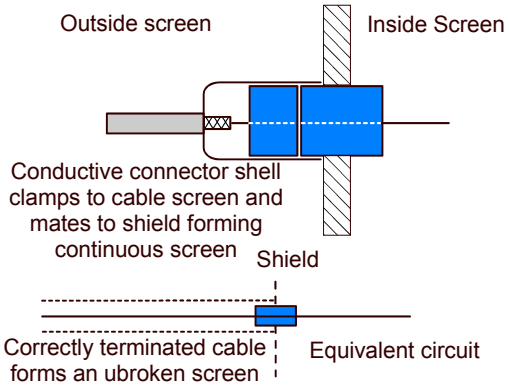




Enclosure

Plastic enclosures -A plastic enclosure can prevent ESD occurring. The weak points are gaps for user interface controls and connectors. ESD will jump through the air gaps to circuitry behind. Make separation enough to prevent ESD or provide a preferred ESD ground path e.g. via metal back-plate. Prevent ESD/EMI entering via cables. Use transient suppressors and filters at cable entry points.

<table>
<tr><td rowspan="2">Shielding, filtering and interface design</td><td>Filters can be used to prevent ESD and conducted EMI entering or leaving via cables or connectors</td><td>Some types of on-board filter:-
• Capacitors - provide simple decoupling. High voltage capacitors may be required to withstand ESD transients
• “Transorb” - Transient suppressors feature fast turn-on and clamping to protect semiconductor devices against ESD
• L-C filters - block transients and EMI entering or leaving
• Series resistors - can attenuate transients and high frequencies - can be used with clamp diodes or decoupling capacitors
• Ferrite beads - attenuate EMI and ESD</td></tr>
<tr><td colspan="2">Design interface circuits to prevent ESD and EMI crossing onto or out of, the system. Connection to ground may be made through a tightly bolted mounting bolt or metal pillar to chassis - make sure no paint, anodisation or coating can impair the ground connection.</td></tr>
<tr><td>Screened cable incorrectly terminated on PCB</td><td>At first sight the screen on this cable may appear reasonably well terminated directly to a ground track. However the ground track is long and thin and crosses the PCB to the ground point. EMI currents have plenty of chance to couple into other circuitry on the PCB. The long ground track presents considerable impedance to the EMI currents.</td><td> 
</td></tr>
<tr><td>R-C filter on I/O line</td><td>Low frequency I/O lines may be filtered using a simple R-C filter circuit. The capacitor should be as close as possible to the connector and connected directly to chassis or RF ground. A similar approach may be taken with a transient suppressor.</td><td> 
</td></tr>
<tr><td>I/O module approach</td><td colspan="2">Filter components may be placed separately on a multilayer I/O module at the connector entry. Connect the ground plane to chassis ground via short low inductance connections - Advantage: The filter may be optimised independently from the design of the remainder of the board.</td></tr>
<tr><td>Filter capacitor types</td><td colspan="2">Decoupling capacitors should have high self resonant frequency
- Low inductance
- Minimise leads and tracks
- Chip capacitor packages can be excellent
Multilayer ceramics are often quoted as being the best for HF decoupling. Polymer dielectric capacitors can have good performance. The capacitor value is often not critical.</td></tr>
</table>

Shielded enclosure	Shields can effectively prevent ESD and EMI radiation entering or leaving a system Make sure it can't get in at cable entry points.	
Incorrectly terminated screened cable	An un-screened connector has been used. The cable screen has been incorrectly terminated in a "pigtail" within the screened enclosure. The pigtail carries EMI currents that will re-radiate within the screen.	
Correctly terminated cable screen	A screened connector been correctly terminated outside the screened enclosure. No EMI currents will enter the screen.	
Circuit design considerations	Hardware can be designed to help give ESD immunity. High impedance lines will be sensitive to fast dV/dt therefore use lower impedances where possible, keep line lengths short and avoid edge triggered circuits. Low impedance loops may pick up fast dI/dt changes -minimise loop sizes.	
Software and firmware considerations	Assume that any port or data line state may be corrupted - design-in ways of detecting fault states. ESD transients are short, so sample states more than once over longer time frame. Design-in safe recovery from possible fault states.	

Key points

- ESD immunity design requires a holistic view
- Remember ESD has high dI/dt and dV/dt and large peak current flow – but is short duration
- Evaluate likely ESD source entry points
- Design enclosure and ground paths to take ESD direct to earth away from susceptible circuitry
- Block ESD/EMI entry at connectors and cables with appropriate filters
- Use hardware/software design to reduce basic susceptibility